

# Silicon Triac

## **2N5573**

15A Triac

200V / 15A

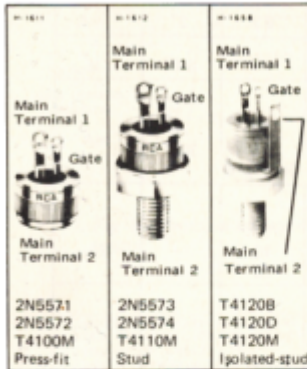
# DATASHEET

OEM –RCA

Source: RCA Databook 1974

## Thyristors

**2N5571 2N5573 T4120B**  
**2N5572 2N5574 T4120D**  
**T4100M T4110M T4120M**



### 15-A Silicon Triacs

Press-Fit, Stud, and Isolated-Stud Type Packages

For 120-V Line Operation – 2N5571, 2N5573, T4120B (40802)\*\*  
 For 240-V Line Operation – 2N5572, 2N5574, T4120D (40803)\*\*  
 For High-Voltage Operation – T4100M, T4110M, T4120M  
 (40797, 40798, 40804)\*\*

\*\* Numbers in parentheses (e.g. 40802) are former RCA type numbers.

**Features:**

- di/dt Capability = 150 A/μs
- Shorted-Emitter Center-Gate Design
- Low On-State Voltage at High Current Levels
- Low Switching Losses
- Low Thermal Resistance

These RCA triacs are gate-controlled, full-wave silicon ac switches. They are designed to switch from an off-state to an on-state for either polarity of applied voltage with positive or negative gate triggering voltages.

These triacs are intended for control of ac loads in applications such as heating controls, motor controls, arc-welding equipment, light dimmers, and power switching systems.

**MAXIMUM RATINGS, Absolute-Maximum Values:**

For Operation with Sinusoidal Supply Voltage at Frequencies up to 50/60 Hz and with Resistive or Inductive Load.

**\*REPETITIVE PEAK OFF-STATE VOLTAGE:**\*

Gate open,  $T_J = -65$  to  $100^\circ\text{C}$  .....

$V_{DROM}$	200	400	600	V
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**\*RMS ON-STATE CURRENT (Conduction angle =  $360^\circ$ ):**

Case temperature  
 $T_C = 80^\circ\text{C}$  (Press-fit & stud types) .....

$T_C = 75^\circ\text{C}$  (Isolated-stud types) .....

For other conditions .....

$I_{T(RMS)}$	15	15	15	A
	See Fig. 3			

**PEAK SURGE (NON-REPETITIVE) ON-STATE CURRENT:**

For one cycle of applied principal voltage  
 \* 60 Hz (sinusoidal) .....

50 Hz (sinusoidal) .....

For more than one cycle of applied principal voltage .....

$I_{TSM}$	100	85	85	A
	See Fig. 4			

**RATE-OF-CHANGE OF ON-STATE CURRENT:**

$V_{DM} = V_{DROM}$ ,  $I_{GT} = 160\text{ mA}$ ,  $t_r = 0.1\ \mu\text{s}$  (See Fig. 13) .....

di/dt	150			A/μs
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**PEAK GATE-TRIGGER CURRENT:**■

For 1 μs max., See Fig. 7 .....

$I_{GTM}$	4			A
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**\*GATE POWER DISSIPATION:**

PEAK (For 1 μs max.,  $I_{GTM} \leq 4\text{ A}$ ; See Fig. 7) .....

AVERAGE .....

$P_{GM}$	16			W
$P_G (AV)$	0.5			W

**\*TEMPERATURE RANGE:**▲

Storage .....

Operating (Case) .....

$T_{stg}$	-65 to 150			$^\circ\text{C}$
$T_C$	-65 to 100			$^\circ\text{C}$

**\*TERMINAL TEMPERATURE (During soldering):**

For 10 s max. (terminals and case) .....

$T_T$	225			$^\circ\text{C}$
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\* In accordance with JEDEC registration data format (JES-14, RDF 2) filed for the JEDEC 2N-Series types.  
 ● For either polarity of main terminal 2 voltage ( $V_{MT2}$ ) with reference to main terminal 1.  
 ■ For either polarity of gate voltage ( $V_G$ ) with reference to main terminal 1.  
 ▲ For temperature measurement reference point, see Dimensional Outline.

**ELECTRICAL CHARACTERISTICS**  
At Maximum Ratings and at Indicated Case Temperature (T<sub>C</sub>) Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	LIMITS			UNITS
		For All Types Unless Otherwise Specified			
		Min.	Typ.	Max.	
Peak Off-State Current: <sup>♣</sup> Gate open, T <sub>J</sub> = 100° C, V <sub>DROM</sub> = Max. rated value	I <sub>DROM</sub>	—	0.2	2*	mA
Maximum On-State Voltage: <sup>♣</sup> For i <sub>T</sub> = 21 A (peak), T <sub>C</sub> = 25° C	V <sub>TM</sub>	—	1.4	1.8*	V
DC Holding Current: <sup>♣</sup> Gate open, Initial principal current = 500 mA (DC), v <sub>D</sub> = 12V: T <sub>C</sub> = 25° C ..... T <sub>C</sub> = -65° C ..... For other case temperatures .....	I <sub>HO</sub>	— —	20 75	75 300*	mA
See Fig. 6					
Critical Rate-of-Rise of Commutation Voltage: <sup>♣</sup> For v <sub>D</sub> = V <sub>DROM</sub> , I <sub>T</sub> (RMS) = 15 A, commutating di/dt = 8 A/ms, gate unenergized, (See Fig. 14): T <sub>C</sub> = 80° C (Press-fit & stud types) ..... = 75° C (Isolated-stud) .....	dv/dt	2* 2	10 10	— —	V/μs
Critical Rate-of-Rise of Off-State Voltage: <sup>♣</sup> For v <sub>D</sub> = V <sub>DROM</sub> , exponential voltage rise, gate open, T <sub>C</sub> = 100° C: 2N5571, 2N5573, T4120B ..... 2N5572, 2N5574, T4120D ..... T4100M, T4110M, T4120M .....	dv/dt	30* 20* 10	150 100 75	— — —	V/μs
DC Gate-Trigger Current: <sup>♣♣</sup> Mode V <sub>MT2</sub> V <sub>G</sub> For v <sub>D</sub> = 12 V (DC), I <sup>+</sup> positive positive R <sub>L</sub> = 30 Ω, III <sup>-</sup> negative negative T <sub>C</sub> = 25° C I <sup>-</sup> positive negative III <sup>+</sup> negative positive	I <sub>GT</sub>	— — — —	20 20 35 35	50 50 80 80	mA
For v <sub>D</sub> = 12 V (DC), I <sup>+</sup> positive positive R <sub>L</sub> = 30 Ω, III <sup>-</sup> negative negative T <sub>C</sub> = -65° C I <sup>-</sup> positive negative III <sup>+</sup> negative positive		— — — —	75 75 100 100	150* 150* 200* 200*	
See Figs. 8 & 9					
DC Gate-Trigger Voltage: <sup>♣♣</sup> For v <sub>D</sub> = 12 V (DC), R <sub>L</sub> = 30 Ω, T <sub>C</sub> = 25° C ..... T <sub>C</sub> = -65° C ..... For other case temperatures ..... For v <sub>D</sub> = V <sub>DROM</sub> , R <sub>L</sub> = 125 Ω, T <sub>C</sub> = 100° C	V <sub>GT</sub>	— — 0.2	1 2 —	2.5 4* —	V
See Fig. 10					
Gate-Controlled Turn-On Time: (Delay Time + Rise Time) For v <sub>D</sub> = V <sub>DROM</sub> , I <sub>GT</sub> = 160 mA, t <sub>r</sub> = 0.1 μs, i <sub>T</sub> = 25 A (peak), T <sub>C</sub> = 25° C (See Figs. 11 & 15)	t <sub>gt</sub>	—	1.6	2.5	μs
Thermal Resistance: Junction-to-Case: Steady-State ..... Transient .....	R <sub>θJC</sub>	—	—	1*	°C/W
See Fig. 12					
Junction-to-Isolated Hex (Stud, see Dim. Outline): Steady-State .....	R <sub>θJIH</sub>	—	—	1.1	

\* In accordance with JEDEC registration data format (JES-14, RDF 2) filed for the JEDEC (2N-Series) types.  
♣ For either polarity of main terminal 2 voltage (V<sub>MT2</sub>) with reference to main terminal 1.  
♣♣ For either polarity of gate voltage (V<sub>G</sub>) with reference to main terminal 1.

File No. 458 2N5571-4; T4100M, T4110M, T4120B, T4120D, T4120M

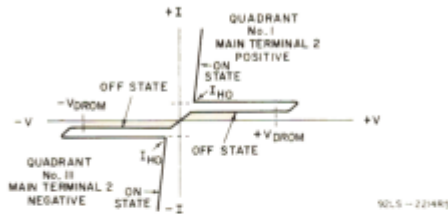


Fig. 1 - Principal voltage-current characteristic.

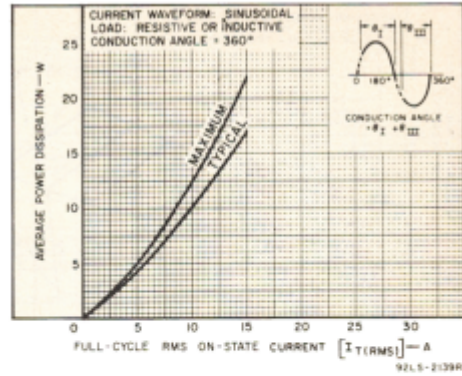


Fig. 2 - Power dissipation vs. on-state current.

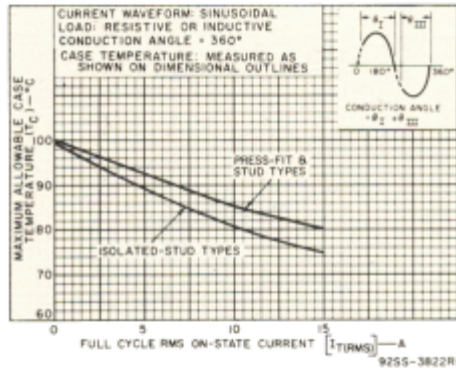


Fig. 3 - Maximum allowable case temperature vs. on-state current.

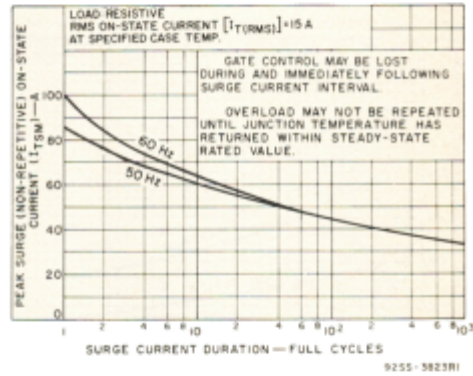


Fig. 4 - Peak surge on-state current vs. surge current duration.

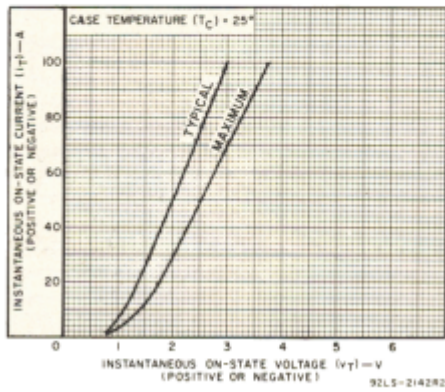


Fig. 5 - On-state current vs. on-state voltage.

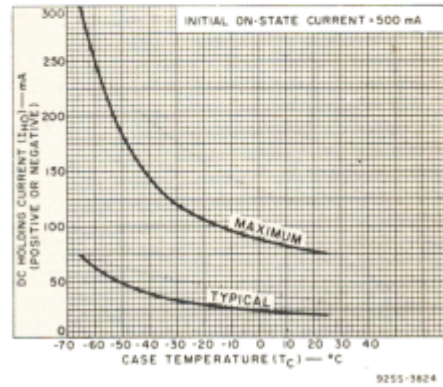


Fig. 6 - DC holding current vs. case temperature.

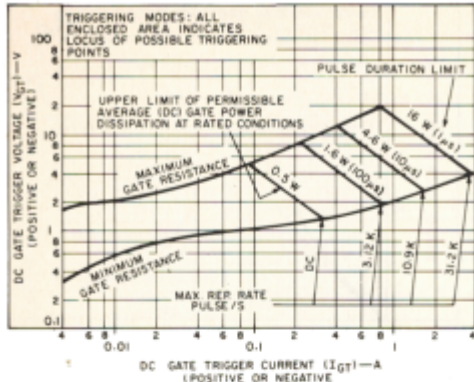


Fig. 7 - Gate trigger characteristics and limiting conditions for determination of permissible gate trigger pulses.

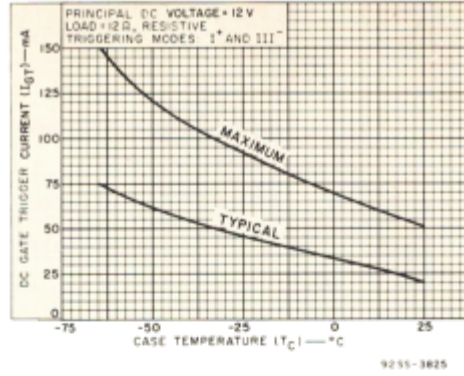


Fig. 8 - DC gate-trigger current vs. case temperature (I\* & III\* modes).

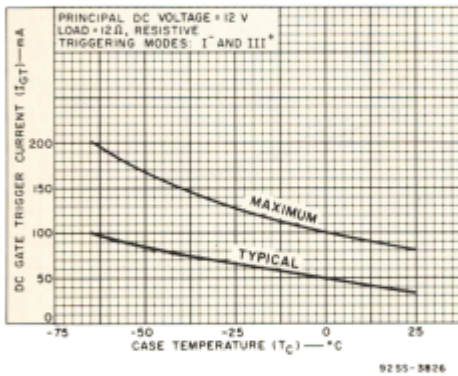


Fig. 9 - DC gate-trigger current vs. case temperature (I\* & III\* modes).

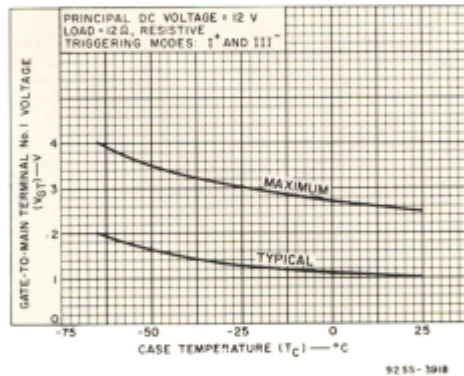


Fig. 10 - DC gate-trigger voltage vs. case temperature.

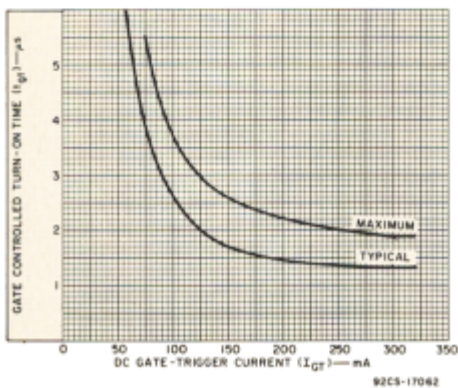


Fig. 11 - Turn-on time vs. gate trigger current.

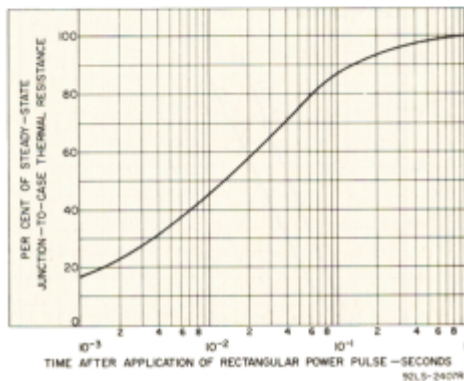


Fig. 12 - Transient junction-to-case thermal resistance vs. time.

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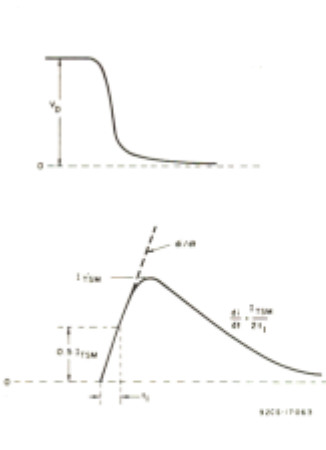


Fig. 13—Rate-of-change of on-state current with time (defining  $di/dt$ ).

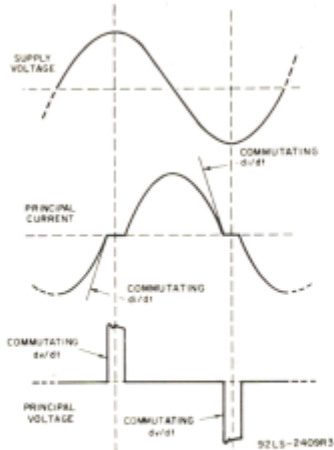


Fig. 14—Relationship between supply voltage and principal current (inductive load) showing reference points for definition of commutating voltage ( $dv/dt$ ).

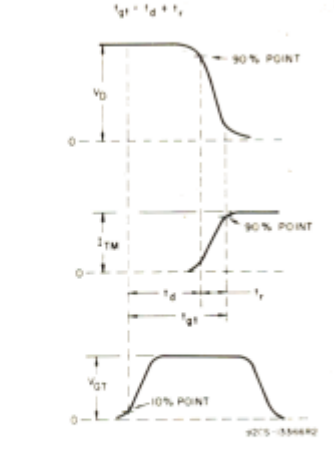


Fig. 15—Relationship between off-state voltage, on-state current, and gate-trigger voltage showing reference points for definition of turn-on time ( $t_{gt}$ ).

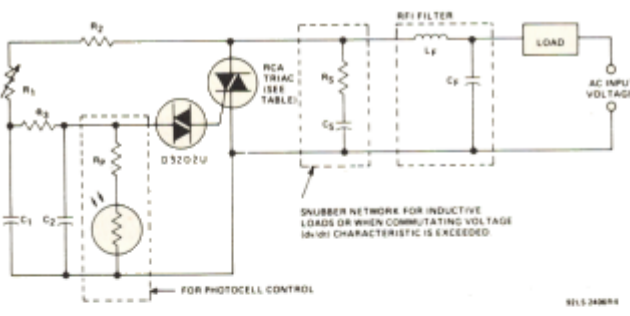


Fig. 16—Typical phase-control circuit for lamp dimming, heat control, and universal-motor speed control.

AC INPUT VOLTAGE	120V 60Hz	240V 60Hz	240V 50Hz
\$C_1\$	0.1μF 200V	0.1μF 400V	0.1μF 400V
\$C_2\$	0.1μF 100V	0.1μF 100V	0.1μF 100V
\$R_1\$	100KΩ 1/2W	200KΩ 1W	250KΩ 1W
\$R_2\$	2.2KΩ 1/2W	3.3KΩ 1/2W	3.3KΩ 1/2W
\$R_3\$	15KΩ 1/2W	15KΩ 1/2W	15KΩ 1/2W
PHOTOCELL CONTROL \$R_P\$	1.2KΩ 2W	1.2KΩ 2W	1.2KΩ 2W
SNUBBER NETWORK \$C_S\$	0.1μF 200V	0.1μF 400V	0.1μF 400V
\$R_S\$	100Ω 1/2W	100Ω 1/2W	100Ω 1/2W
RFI FILTER \$C_F\$	0.1μF 200V	0.1μF 400V	0.1μF 400V
\$L_F\$	100μH	200μH	200μH
RCA TRIACS	2N5567 2N5568 T4120B	2N5568 2N5570 T4120D	2N5568 2N5570 T4120D

\*Typical values for lamp dimming circuits.

**MOUNTING CONSIDERATIONS**

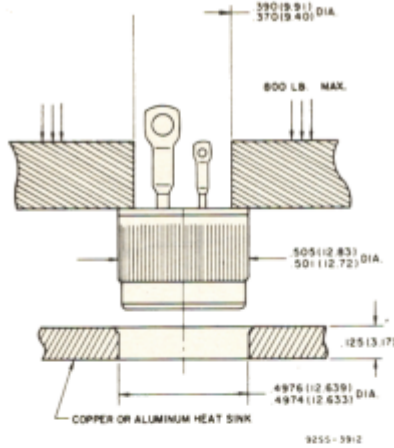
Mounting of press-fit package types depends upon an interference fit between the thyristor case and the heat sink. As the thyristor is forced into the heat-sink hole, metal from the heat sink flows into the knurl voids of the thyristor case. The resulting close contact between the heat sink and the thyristor case assures low thermal and electrical resistances.

A recommended mounting method, shown in Fig. 17, shows press-fit knurl and heat-sink hole dimensions. If these dimensions are maintained, a "worst-case" condition of 0.0085 in. (0.2159 mm) interference fit will allow press-fit insertion below the maximum allowable insertion force of 800 pounds. A slight chamfer in the heat-sink hole will help

center and guide the press-fit package properly into the heat sink. The insertion tool should be a hollow shaft having an inner diameter of 0.380 ± 0.010 in. (9.65 ± 0.254 mm) and an outer diameter of 0.500 in. (12.70 mm). These dimensions provide sufficient clearance for the leads and assure that no direct force will be applied to the glass seal of the thyristor.

The press-fit package is not restricted to a single mounting arrangement; direct soldering and the use of epoxy adhesives have been successfully employed. The press-fit case is tin-plated to facilitate direct soldering to the heat sink. A 60-40 solder should be used and heat should be applied only long enough to allow the solder to flow freely.

2N5571-4; T4100M, T4110M, T4120B, T4120D, T4120M \_\_\_\_\_ File No. 458



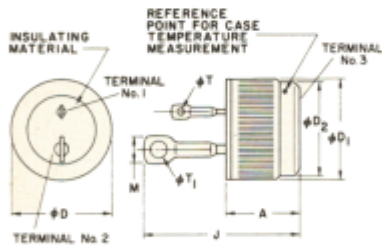
NOTE: Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated.

Fig. 17—Suggested mounting method for press-fit package types.

Table I — Case-to-Heat Sink Thermal Resistance for Different Mounting Arrangements.

Package	Type of Mounting Employed	Thermal Resistance-°C/W
Press-Fit	Press-fitted into heat sink. Minimum required thickness of heat sink = 1/8 in. (3.17 mm)	0.5
	Soldered directly to heat sink. (60-40 solder which has a melting point of 188° C should be used. Heating time should be sufficient to cause solder to flow freely).	0.1 to 0.35
Stud & Isolated-Stud	Directly mounted on heat sink with or without the use of heat-sink compound.	0.6
Stud	Mounted on heat sink with a 0.004 to 0.006 in. (0.102 to 0.152 mm) thick mica insulating washer used between unit and heat sink.	2.5
	Without heat sink compound With heat sink compound	1.5

DIMENSIONAL OUTLINE FOR TYPES  
2N5573, 2N5574, T4110M



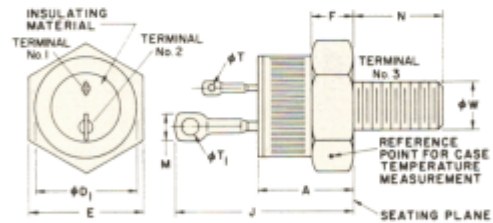
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	.380	—	9.65	2
phi D	.501	.510	12.73	12.95	
phi D1	—	.505	—	12.83	1
phi D2	.465	.475	11.81	12.07	
J	—	.750	—	19.05	1
M	—	.155	—	3.94	
phi T	.058	.068	1.47	1.73	1
phi T1	.080	.090	2.03	2.29	

NOTE 1: Contour and angular orientation of these terminals is optional.

NOTE 2: Outer diameter of knurled surface.

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DIMENSIONAL OUTLINE FOR TYPES  
2N5571, 2N5572, T4100M



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	.330	.505	8.4	12.8	—
phi D1	—	.544	—	13.81	—
E	.544	.562	13.82	14.28	—
F	.113	.200	2.87	5.08	3
J	—	.950	—	24.13	—
M	—	.155	—	3.94	1
N	.422	.453	10.72	11.50	—
phi T	.058	.068	1.47	1.73	—
phi T1	.080	.090	2.03	2.29	—
phi W	.2225	.2268	5.652	5.760	2

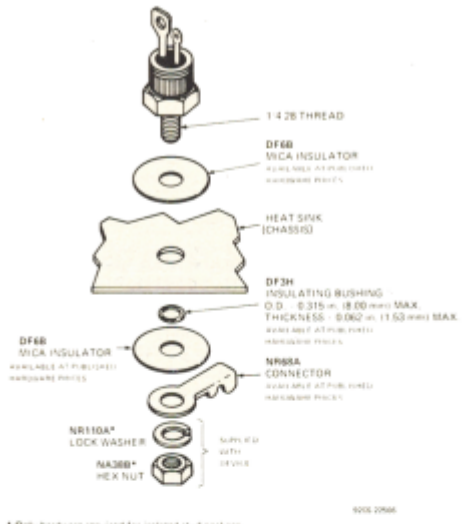
NOTE 1: Contour and angular orientation of these terminals is optional.

NOTE 2: Pitch diameter of 1/4-28 UNF-2A (coated) threads (ASA B1.1-1960).

NOTE 3: A chamfer or undercut on one or both ends of hexagonal portion is optional.

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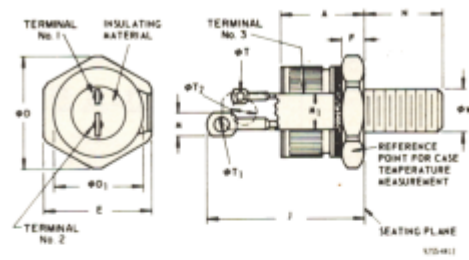
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\* Only hardware required for isolated stud package.  
 In the United Kingdom, Europe, Middle East, and Africa, mounting hardware policies may differ; check the availability of all items shown with your RCA sales representative or supplier.

Fig. 18—Suggested mounting arrangement for stud and isolated-stud package types.

DIMENSIONAL OUTLINE FOR TYPES T4120B, T4120D, T4120M



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	.673	—	17.09	
phi D	.604	.614	15.34	15.59	
phi D <sub>1</sub>	.501	.506	12.72	12.82	
E	.551	.557	13.99	14.14	
F	.175	.185	4.44	4.69	
J	—	1.055	—	26.79	
M	—	.155	—	3.94	
M <sub>1</sub>	.200	.210	5.08	5.33	
N	.422	.452	10.72	11.48	
phi T	.058	.068	1.47	1.73	2
phi T <sub>1</sub>	.080	.090	2.03	2.29	2
phi T <sub>2</sub>	.138	.148	3.50	3.75	2
phi W	.225	.2268	5.652	5.760	3

NOTE 1: Ceramic between hex (stud) and terminal No.3 is beryllium oxide.  
 NOTE 2: Contour and angular orientation of these terminals is optional.  
 NOTE 3: Pitch diameter of 1/4-28 UNF-2A (coated) threads (ASA B1. 1-1960).

**TERMINAL CONNECTIONS**  
 Terminal No.1—Gate  
 Terminal No.2—Main Terminal 1  
 Case, Terminal No.3—Main Terminal 2